UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/733,751 | 12/11/2003 | Jonson C. Au | 02-6221 1496.00289 | 8406 |

24319 7590 06/11/2007

LSI LOGIC CORPORATION
1621 BARBER LANE
MS: D-106
MILPITAS, CA 95035

| EXAMINER | |
|---|---|
| BAE, JI H | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2115 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 06/11/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/733,751 | AU, JONSON C. | |
| | Examiner | Art Unit | |
| | Ji H. Bae | 2115 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *22 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 16-21* is/are rejected.

7)☒ Claim(s) *15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 14 February 2007 has been entered.

### *Response to Arguments*

Applicant's arguments filed on 14 February 2007 have been fully considered but they are not persuasive.

The examiner notes that applicant has amended the claims so as to further define over the cited prior art, and has also provided additional argument to support the claims. In the first paragraph on page 10 of the remarks, applicant alleges that the combination of Keskar and Dorst does not anticipate the applicant's claims because neither Keskar nor Dorst teaches an interface circuit having a second bus interface unit to communicate on the system bus. The examiner does not agree with the applicant's assertion. Referring to Keskar, Fig. 2, Keskar clearly teaches a processor [execution unit 24] having a first bus interface unit [BIU 26] to communicate on a system bus [address, data, and control signals], and an interface circuit [memory interface 66] having a second bus interface unit [high speed interface 64] to communicate on the system bus.

The applicant also alleges that neither Keskar nor Dorst teaches a processor configured to operate at a first data rate in response to a first clock signal and the interface circuit configured to operate at a second data rate in response to a second clock signal. Applicant

alleges that Keskar and Dorst are silent as to the two claimed clock signals. The examiner respectfully disagrees with the applicant's assertion. Keskar clearly teaches that the execution operates at one speed, while the memory interface operates at a second speed which is typically slower than the processor speed [col. 3, lines 55-59]. Based on other parts of the disclosure, it is clear that clock speeds are in view [col. 5, lines 33-42, fast processor clock speed and slower memory clock speed]. In light of this, the applicant's amendments are not sufficient to define over the combination of Keskar and Dorst, and the examiner maintains the grounds of rejection presented in the previous office action.

Regarding claim 3, Keskar clearly teaches that the SDRAM clock signal (i.e. the "second clock signal") is generated in response to the processor clock signal (i.e. the "first clock signal") [col. 20, lines 15-19, processor clock divided down to produce the memory clock]. Moreover, Keskar clearly teaches that the memory interface (i.e. the "interface circuit") operates at the speed of the SDRAM memory [col. 3, lines 55-59].

Regarding claim 13, the examiner's reference to a "missing element" is based not on the applicant's claims or disclosure, but on Ghaffari's disclosure. Ghaffari broadly teaches that a DMA engine "waits" until the system is ready for a DMA transaction, but is silent as to the mechanics of how the wait function would be implemented. In light of Tanaka's teaching regarding the implementation of a status bit that is set when a DMA operation completes, the examiner submits that one of ordinary skill in the art would have readily observed the applicability of Tanaka's implementation to the wait function of Ghaffari.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 16-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 16, the claim recites that the lower bound register is set "depending on whether said apparatus is performing the read/write operation to/from said first memory". It is unclear whether the applicant intends to claim that the lower bound register is set depending on whether any operation is performed at all (read or write), or if the applicant intends to claim that the lower bound register is set to a value corresponding to a read operation or a write operation.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dorst, U.S. Patent No. 6,941,416 B2, in view of Keskar et al., U.S. Patent No. 6,366,989 B1.

Regarding claim 1, Dorst teaches an apparatus comprising:

a memory having a plurality of banks coupled to a memory controller configured to precharge and close all of said plurality of banks prior to a refresh cycle being performed [col. 8, lines 18-28].

Dorst does not teach an interface circuit with a state machine for converting data received at a first data rate to a second data rate.

Keskar teaches an apparatus comprising:

a processor configured to operate at a first data rate response to a first clock signal [Fig. 2, execution unit 24, col. 5, lines 33-42, fast processor clock], **and having a first bus interface unit [BIU 26] to communicate on a system bus [address/data/control lines 68/70/72];**

an interface circuit [Fig. 2, memory interface 66 a.k.a. "low speed interface"] having a state machine and **a second bus interface unit [Fig. 2, high speed interface 64] to communicate on said system bus,** said interface circuit being configured to operate at a second data rate in response to a second clock signal [col. 3, lines 55-59, col. 5, lines 33-42, slower memory clock], and convert data received from said processor over a system bus from said first data rate to said second data rate [col. 1, line 64-67, col. 5, lines 33-42, col. 22, lines 16-20].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Dorst and Keskar by modifying Dorst to implement the low/high speed memory interface of Keskar. Both Dorst and Keskar are directed towards memory interfaces for synchronous dynamic random access memories. The teachings of Keskar would improve the system of Dorst by providing a way to reduce the latency between the CPU and the memories, thus improving overall system performance [Keskar, col. 2, lines 1-14].

Regarding claim 2, it would have been obvious to one of ordinary skill in the art to generate the clocks independently as a matter of design choice.

Regarding claim 3, Keskar teaches that the second clock signal is generated in response to the first clock signal [col. 20, lines 15-19].

Regarding claim 4, Keskar teaches that the state machine is configured to control the conversion between the first and second data rate.

Regarding claim 5, Dorst teaches that the memory controller provides paging to the memory [col. 8, lines 3-4].

Regarding claim 6, Dorst teaches that the processor may comprise a memory controller [Fig. 2], wherein the memory controller is capable of communicating with an SDRAM memory and CSI memory [Fig. 4 and 5].

Regarding claim 7, it would have been obvious to one of ordinary skill in the art to utilize a bi-directional FIFO to transfer data between the circuits as a matter of design choice. FIFOs are frequently used in the art to buffer data between digital circuits.

Regarding claim 9, Dorst teaches that the memory controller is configured to minimize access requests to the memory. The paging scheme of Dorst allows an SDRAM transaction without first having to activate the row based on a previous transfer [col. 8, lines 6-9].

Regarding claims 10 and 11, Keskar/Dorst teaches the apparatus of claim 1. Keskar/Dorst also teaches the method implemented by the claimed apparatus, and the apparatus with means to achieve the functionality of the claimed apparatus.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dorst/Keskar as applied to claims 1-11 above, and further in view of Ghaffari, U.S. Patent No. 7,130,932 B1.

Regarding claim 12, Keskar/Dorst does not teach a DMA engine.

Ghaffari teaches a DMA engine that waits until the system is ready for a DMA transaction [col. 10, lines 23-39].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Keskar/Dorst with Ghaffari by implementing the DMA engine of Ghaffari in the system of Keskar/Dorst. DMA provides the advantage of being able to transfer data from memory to other devices without processor involvement, thus freeing host resources for other uses [Ghaffari, col. 2, lines 5-14].

Claims 13, 14, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dorst/Keskar/Ghaffari as applied to claim 12 above, and further in view of Cheng et al., U.S. Patent No. 6,606,689 B1.

Regarding claims 13 and 14, Dorst/Keskar/Ghaffari does not teach a completion bit.

Cheng teaches a system with a DMA controller that employs a busy bit. The busy bit is set when a DMA transaction is occurring, and cleared when it is completed [col. 12, lines 63-67].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Keskar/Dorst/Ghaffari and Cheng by implementing the DMA control register with a busy bit as taught by Cheng. Although Keskar/Dorst/Ghaffari generally teaches waiting for a DMA ready state, none of the disclosures teach a specific implementation for how such a ready state would be verified. In light of the silence of the disclosures as to how to implement a waiting function, and in light of Cheng's teaching of a busy bit which provides such a capability, it would have been obvious to one of ordinary skill in the art to modify the combination in light of Cheng's teaching.

Regarding claim 21, Cheng further teaches that the control register implements a bit that specifies the direction of the DMA transfer [col. 12, lines 59-61].

***Allowable Subject Matter***

Claim 15 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ji H. Bae whose telephone number is 571-272-7181. The examiner can normally be reached on Monday-Friday, 10 am to 6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ji H. Bae
Patent Examiner
Art Unit 2115
ji.bae@uspto.gov
571-272-7181

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100